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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,601	03/20/2001	Tetsuji Kishi	60188-045	9328

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EXAMINER
NGUYEN, HAU H

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 06/26/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,601	KISHI ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 9-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Fukushima et al. (U.S. Patent No. 5,507,026).

Referring to claims 1, 9-11, Fukushima et al. teach a graphic processor, which as shown in Fig. 3, comprises a first interface 105, for receiving externally input graphics commands through buses 12, 30 and 32; a second interface 106 performing data transfer operation to and from a frame buffer via buses 11, 12, and 32; a data bus between the first and second interfaces; a drawing processing unit 101 (display data generation section) for decoding a drawing command sent from the system bus interface 105 through the data bus (col. 10, lines 5-9); a CRT control unit 104 outputs synchronization signals via the local bus interface 106 to the CRT display unit 207 (please see also to Fig. 1) (col. 11, lines 6-10); and a bus control unit 103 for performing arbitration with the bus arbitrator 202 externally provided with the graphic processor 100 via the system bus interface 105 in order to acquire a bus priority of the system bus 211 (col. 11, lines 1-5).

Fukushima et al. further teach the drawing processing unit 101 decodes a drawing command sent from the system bus interface 105 in order to check whether data to be processed is in the frame buffer or in the main memory, and also calculates an address of this data to be

processed (col. 10, lines 5-18). Fig. 5 shows an address translation mechanism, wherein a check is made whether 20 bits of the directory 233 and page 234 (first data storage) are coincident with 32 pieces of 20-bits tags of the address translation table (TLB) 242 (second data storage) with the memory management unit 102. If there is an entry where the tag is coincident with 20 bits, 20 bits of the page address of this entry is summed with 12 bits of the offset of the virtual address 221, which becomes a 32-bit physical address 236. If there is no entry having a tag coincident with the upper 20 bits of the virtual address 221 in the address translation table 242, an entry in which the upper 20 bits of the virtual address 221 is used as a tag is newly formed (writing new data). At this time, the corresponding page table entry 228 is read out with reference to the page directory 223 and page table 224 on the main memory 203 by employing the directory 233 by employing the directory 233 and page 234 of the virtual address 221, and is equal to a page address and attribute of an entry newly formed in the address translation table 242, so that it can be translated into the physical address 236.

In regard to claim 10, as shown in Figs. 1 and 3, external bus is connected from the CPU 201 to the first interface 105, frame buffer 205 is connected to the second interface 106, and a display device 207 is coupled to the CRT control unit 104.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukushima et al. (U.S. Patent No. 5,507,026) in view of Chee (U.S. Patent No. 6,204,864).

Referring to claims 2 and 3, as applied to claim 1 above, Fukushima et al. teach all the limitations of claim 2, except that the bus control section sets a priority for each of at least: a data transfer operation of transferring an externally-input graphics command to the work memory; a data transfer operation of supplying a graphics command from the work memory to the display data generation section; and a data transfer operation of supplying display data from the work memory to the image display section, and the setting of priorities of data transfer operations can be changed dynamically.

However, Chee teaches a video display controller 36 (seen in Fig. 5) having a first host interface 48 programmable to configure the VDC 36 for interface with a number of conventional bus configurations (col. 7, lines 27-30), a second interface 62 coupled with a DRAM controller 58. The functional block diagram of the DRAM controller 58, as depicted in Fig. 7, is coupled to receive requests for accessing DRAM 38 by a CPU 74, frame memory 72, or display FIFO 78. The DRAM controller 58 comprises a sequencer and controller 86 including a priority logic unit 90 (bus control section) implementing a logical selection process among the pending requests for access to the DRAM 38. As shown in Fig. 8, pending requests for access to the DRAM 38 are first of all assigned to one of two tiers (an upper tier and a lower tier). Within the upper tier, pending requests are ranked in order of priority (numbered 1u through 5u). Similarly, within the lower tier, pending requests are ranked in order of priority (indicated as 1l through 3l) (col. 11, lines 1-22). Chee further teaches the set of priorities are assigned dynamically (col. 14, lines 46-48).

Therefore, it would have been obvious to one skilled in the art to utilize the method of request handling in a graphics processor as taught by Chee in combination with the graphics processor as taught by Chee in order to reduce access delay for other devices that also need quick access (col. 5, lines 37-38).

In regard to claims 4-8, Fukushima et al. further teach the drawing processing unit 101 decodes a drawing (plotting) command sent from the system bus interface 105 in order to check whether data to be processed is in the frame buffer or in the main memory, and also calculates an address of this data to be processed (col. 10, lines 5-18). Thus, Fukushima et al. teach all the limitations of claims 4-8 except for a processing amount estimating section for estimating a data processing amount at the display data generation section based on a result of the pre-decoding by the pre-decoding section, wherein the bus control section changes the priorities of the data transfer operations according to the data processing amount estimated by the processing amount estimating section.

However, as shown in Fig. 6, Chee teaches the assignment of priority is dependent upon the data level of the FIFO. Specifically, one of these pointers (pointer 66) indicates that when the data level in the FIFO falls below this pointer, then a FIFOLO request is issued for additional data from the DRAM. The other pointer 68 indicates the issuance of a FIFOHI request for additional data from the DRAM 38 (col. 9, lines 16-20). As cited above, the assignment of priorities are depicted in Fig. 8. Chee further teaches the half-frame buffer issues requests for access to the DRAM on a FRAMELO (low priority), or FRAMEHI (high priority) basis dependent upon the amount of data remaining in the limited memory capacity of the half-frame buffer for use in refreshing pixels of the LCD 24 (col. 10, lines 21-26).

Therefore, it would have been obvious to one skilled in the art to utilize the method of request handling in a graphics processor as taught by Chee in combination with the graphics processor as taught by Chee in order to reduce access delay for other devices that also need quick access (col. 5, lines 37-38).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

Chee et al. (U.S. Patent No. 5,767,866) teach a Video display controller (VDC) having a sequencer and controller (SEQC) arbitrating access to a dynamic random access memory (DRAM) of the VDC among a CPU, a video memory of the first-in-first-out (FIFO) type, a bit-BLT, and other devices of the computer system.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

06/23/2003

Matthew C. Bella

MATTHEW C. BELLA
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